15-17, 20-21, 31, 34-35, 38-39

DERWENT-ACC-NO: 2000-369267

DERWENT-WEEK: 200032

TITLE: Semiconductor device manufacturing method involves forming SOG film at middle of trench and then forming HTO film at its upper surface by CVD

Hideaki

PATENT-ASSIGNEE: NEC CORP[NIDE]

PRIORITY-DATA: 1998JP-0281574 (October 2, 1998)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2000114362 A	April 21, 2000	N/A	005	H01L 021/76

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP2000114362A	N/A	1998JP-0281574	October 2, 1998

INT-CL (IPC): H01L021/316, H01L021/318 , H01L021/76

ABSTRACTED-PUB-NO: JP2000114362A

BASIC-ABSTRACT:

NOVELTY - Upper portion of trench is implanted with HTO film (6) by CVD, after embedding SOG film (5) at the middle of trench, in depth direction.

USE - For trench formation in manufacture of semiconductor device.

ADVANTAGE - Attains favorable trench shape by wet etching and high efficient trench isolation by sufficient embedding of HTO films, hence trench with high aspect ratio is obtained.

DESCRIPTION OF DRAWING(S) - The figure shows process sectional view of semiconductor device manufacture.

SOG film 5

HTO film 6

CHOSEN-DRAWING: Dwg.2/6

TITLE-TERMS: SEMICONDUCTOR DEVICE MANUFACTURE METHOD FORMING SOG FILM MIDDLE TRENCH FORMING FILM UPPER SURFACE CVD

DERWENT-CLASS: L03 U11

CPI-CODES: L04-C07C; L04-C12C;

EPI-CODES: U11-C05B5; U11-C05B7; U11-C08A2;

SECONDARY-ACC-NO:

CPI Secondary Accession Numbers: C2000-112023

Non-CPI Secondary Accession Numbers: N2000-276464

MANUFACTURE OF SEMICONDUCTOR DEVICE

Patent Number: JP2000114362
Publication date: 2000-04-21
Inventor(s): ONISHI HIDEAKI
Applicant(s): NEC CORP
Requested Patent: JP2000114362
Application Number: JP19980281574 19981002
Priority Number(s):
IPC Classification: H01L21/76; H01L21/316; H01L21/318
EC Classification:
Equivalents:

Abstract

PROBLEM TO BE SOLVED: To prevent degradation in shape due to wet etching during a device process, by filling element isolation trenches partway in the direction of the depth of the trenches by SOG, and filling the upper part of the trenches with an oxide film by CVD when the trenches are filled with an oxide film.
SOLUTION: A SiO2 film 2 is formed on a Si substrate 1 by thermal oxidation, and a SiN film 3 is formed on the SiO2 film 2. The SiN film 3, SiO2 film 2, and Si substrate 1 are anisotropically etched, respectively, to form isolating trenches. An SiO2 film 4 is formed in the trenches, a SOG solution is then applied, and the trenches are filled by SOG partway in the direction of the depth of the trenches to form a SOG film 5. Subsequently, the upper part of the interior of the trenches is subjected to CVD at a high a temperature as 800 deg.C or so using silane gas, an HTO film 6 forming an oxide film is thereby formed, and the trenches are filled.

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特開2000－114362
（P2000－114362A）
(43)公開日　平成12年４月21日(2000.4.21)

(51)Int.Cl.'	識別記号	FI		テーマコード'（参考）
H01L 21/76		H01L 21/76	L	5F032
21/316		21/316	H	5F058
21/318		21/318	B	

審査請求　有　請求項の数３　ＯＬ　（全５頁）

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(22)出願日　平成10年10月２日(1998.10.2)

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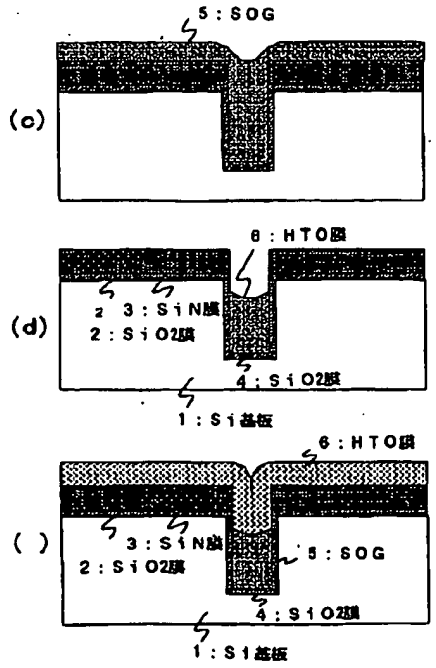
AA77 AA78 DA02 DA10 DA23
DA25 DA33 DA34 DA53
5F058 BA02 BD02 BD04 BD10 BD19
BF02 BF07 BF23 BF29 BF46
BH12 BH20 BJ01 BJ06

(54)【発明の名称】　半導体装置の製造方法

(57)【要約】　（修正有）
【課題】　半導体装置のトレンチ分離において、ＳＯＧ膜でトレンチの埋込を行うと、デバイスプロセス中のウエットエッチング工程により大きくエッチングされ、トレンチ分離の形状が悪化する。
【解決手段】　トレンチ素子分離工程を有する半導体装置の製造方法において、トレンチ素子分分離の酸化膜による埋め込みを行う際、トレンチの深さ方向の途中までＳＯＧで埋め込み、トレンチの上部は、ＣＶＤによる酸化膜としてＳｉＯ$_2$膜例えばＨＴＯ膜により埋め込みを行う。



【特許請求の範囲】
【請求項１】　トレンチ分離形状を有する半導体装置の製造方法において、トレンチ素子分分離の酸化膜による埋め込みを行う際、トレンチの深さ方向の途中までＳＯＧで埋め込み、トレンチの上部は酸化膜により埋め込みを行うことを特徴とする半導体装置の製造方法。
【請求項２】　前記トレンチの上部の酸化膜が、ＨＴＯ膜またはＬＴＯ膜である請求項１に記載の方法。
【請求項３】　前記ＳＯＧ膜が、無機ＳＯＧ膜、有機ＳＯＧ膜、またはＨＳＱ（Hydrogen-Silsesquioxane）膜である請求項１に記載の方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、トレンチ分離工程を有する半導体装置の製造方法に関し、詳しくは、良好なトレンチ分離形状が得られるように改良された半導体装置の製造方法に関する。
【０００２】
【従来の技術】本発明が関する半導体装置の製造方法では、良好なトレンチ分離形状が得られることが重要な要素の一つとなっている。
【０００３】この目的のために、通常埋め込み性が比較的良く、熱酸化膜に近い膜質のトレンチ埋め込み酸化膜を得る方法として、ＨＤＰ－ＣＶＤを用いる方法がある。しかしながら、この方法では、トレンチ分離幅２００ｎｍ以下でアスペクト比３以上の高アスペクト比のトレンチの埋め込みを行うと、図５の様に十分な埋め込み性が得られず、素子分離特性の悪化を招くことになる。
【０００４】また埋め込み性良く酸化膜を形成する方法としては、塗布膜であるＳＯＧを用いて酸化膜を形成する方法がある。この方法によれば、上記のような高アスペクト比のトレンチの埋め込みが可能となるが、図６に示すように、トレンチと他の部分との間に大きい段差が生じるという欠点がある。
【０００５】さらに特公平７－０７７２３１号公報には、半導体装置のトレンチ分離方法が開示されている。この公知の方法においては、アスペクト比の大きいトレンチを隙間なく埋め込むために、基板上に下敷酸化膜、窒化膜を成長後、それらの膜にトレンチパターンを開口し、窒化膜をマスクにトレンチを掘削し、トレンチ表面を酸化した後、ＳＯＧを塗布、エッチバックし、トレンチ表面近くまでＳＯＧがトレンチを埋め込む構造とする。その後、ウェットエッチング耐性の良いＨＴＯ膜をＣＢＤにより成長させ、初期に設けた酸化膜、窒化膜を除去し、基板表面を酸化することにより、トレンチ分離を有する、段差の小さい基板が得られる。
【０００６】
【発明が解決しようとする課題】しかしＳＯＧ膜は、ウエットエッチング耐性が弱いために、デバイスプロセス中のウエットエッチング工程により、図３のように大きくエッチングされ、トレンチ分離の形状が悪化し、素子特性に悪影響を及ぼす。またＳＯＧ膜は金属等の不純物を多く含む膜であり、トレンチ表面にＳＯＧ膜がむき出しの状態では、ゲート酸化工程等への悪影響を及ぼすおそれがある。
【０００７】本発明の主な目的は、埋め込み性の良いトレンチ分離を形成する半導体装置の製造方法を提供することにある。
【０００８】本発明の他の目的は、エッチング耐性が強いトレンチ分離を形成し、プロセス安定性の高い半導体装置の製造方法を提供することにある。
【０００９】
【課題を解決するための手段】本発明の特徴は、トレンチ素子分離の埋め込み工程において、トレンチの深さ方向の途中までＳＯＧを用いた酸化膜を形成し、トレンチの上部の埋め込みはＣＶＤ法による酸化膜で形成することにある。
【００１０】すなわち本発明による製造方法においては、トレンチ素子分分離の酸化膜による埋め込みを行う際、トレンチの深さ方向の途中までＳＯＧで埋め込み、トレンチの上部は、ＣＶＤによる酸化膜としてＳｉO_2膜例えばＨＴＯ膜により埋め込みを行う。
【００１１】このようにＳＯＧを用いてトレンチ上部の埋め込みを行うことにより、アスペクト比の高いトレンチの埋め込みを行うことが容易となり、かつトレンチ上部の埋め込みを膜質、特にウエットエッチング耐性の良いＨＴＯ膜等のＣＶＤ膜で形成することで、デバイスプロセス中でのウエットエッチングによる形状悪化を防ぐ役目を果たす。
【００１２】従って、埋め込み性が良くかつプロセス安定性の高いトレンチ分離がアスペクト比が高いトレンチでも実現出来るという効果が得られる。
【００１３】
【発明の実施の形態】本発明を図面を参照して説明する。図１（ａ）乃至図４（ｊ）は、本発明の一実施の形態における工程断面図を示している。
【００１４】まず、Ｓｉ基板１上に、熱酸化によりＳｉO_2膜２を例えば１０ｎｍの厚さで形成し、ＣＶＤ法によりＳｉＮ膜３を例えば１５０ｎｍの厚さで形成する。そしてリソグラフィー工程を用いてＳｉＮ膜３、ＳｉO_2膜２、Ｓｉ基板１をそれぞれ異方性エッチングによりエッチングし、トレンチ分離の溝を例えば幅２００ｎｍ、深さ５００ｎｍで形成する（図１（ａ））。
【００１５】そしてエッチングダメージ緩和のために、熱酸化によりトレンチ内部にＳｉO_2膜４を形成する（図１（ｂ））。
【００１６】ついでＳＯＧ溶液を塗布し、例えば４００℃でベークを行ってＳＯＧ膜５を形成する（図２（ｃ））。ＳＯＧ膜５は、このように溶液を塗布することにより形成するので、本例の様なアスペクト比の高い

トレンチ内部にも埋め込み性良く膜形成できる。次にSi基板表面から100nm程度の深さまで、異方性ドライエッチングによりSOG膜5のエッチバックを行う（図2（d））。

【0017】次に、トレンチの溝の上部100nmを、シラン系ガスを用いて800℃程度の高温でCVDを行うことにより、酸化膜形成を行うことによる、いわゆるHTO膜6を200nmの厚さで形成することにより埋め込みを行う（図2（e））。

【0018】このHTO膜6は、ウエットエッチング耐性も高く、かつ金属不純物等が混入しにくいことで知られている。そしてCMPにより、SiN上の余分なHTO膜6は除去される（図3（f））。

【0019】ついで、ウェットエッチングにより、SiN膜3とSiO_2膜2を除去し（図3（g））、熱酸化によりウェルやチャネル形成のイオン注入のマスクとなるSiO_2膜7を形成し（図3（h））、そして図では簡単のため省略するが、イオン注入でウェルとチャネルを形成した後に、ウエットエッチングでSiO_2膜7を除去し（図4（i））、熱酸化によりゲートSiO_2膜8が、そして例えばCVD法によるポリシリコンでゲート電極9が形成される（図4（j））。

【0020】この後は、公知の方法でゲート電極のパターニングが行われ、ソース・ドレインが形成され、配線工程を経てMOSデバイスが形成されることになる。

【0021】このような製造方法においては、トレンチの下部はSOGで埋め込み、上部はCVD法で例えばHTO膜で埋め込んでいるため、本例のようなアスペクト比の高いトレンチでも良好に埋め込むことができ、かつウエットエッチング耐性の高いHTO膜で覆っているので、プロセス中のトレンチ酸化膜の膜減りも小さく、このため良好なトレンチ形状が得られる。さらに、SOGがキャップされるために、SOG中の不純物のゲート酸化工程等への影響も防ぐことが出来るという効果がもたらされる。これにより、ウエットエッチング耐性の高い膜を形成することができる。

【0022】上記の実施の形態において、HTO膜の代わりに、ウエットエッチング耐性の高さが得られるならば、成長温度を低くした、いわゆるLTO膜を用いても良い。またプラズマCVDでも、HDP（High Density Plasma）CVDで形成した酸化膜は、ウエットエッチング耐性の高い膜が得られることが知られており、HTOの代わりにこれを用いても良い。さらにSOG膜は、無機SOG、有機SOGのれを用いても良く、HSQ（Hydrogen-Silsesquioxane）の様な低誘電率の塗布膜を用いても良い。

【0023】

【発明の効果】以上に説明したように、本発明の半導体装置の製造方法においては、SOGを用いてトレンチ上部の埋め込みを行うことにより、アスペクト比の高いトレンチの埋め込みを行うことが容易となり、かつトレンチ上部の埋め込みを膜質、特にウエットエッチング耐性の良いHTO膜等のCVD膜で形成することで、デバイスプロセス中でのウエットエッチングによる形状悪化を防ぐ役目を果たす。

【0024】従って、埋め込み性が良くかつプロセス安定性の高いトレンチ分離がアスペクト比が高いトレンチでも実現出来るという効果が得られる。

【図面の簡単な説明】

【図1】（a），（b）は本発明の一実施の形態における工程断面図。

【図2】（c）～（e）は図1（a）の工程に続いて行われる工程の工程断面図。

【図3】（f）～（h）は図2（e）の工程に続いて行われる工程の工程断面図。

【図4】（i），（j）は図3（h）の工程に続いて行われる工程の工程断面図。

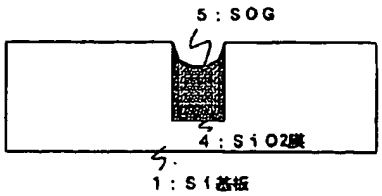
【図5】従来の方法で得られたトレンチ埋め込み酸化膜を示す断面図。

【図6】従来の他の方法で得られたトレンチ埋め込み酸化膜を示す断面図。

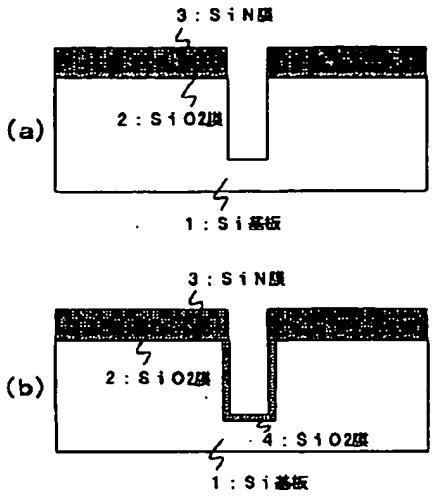
【符号の説明】

1　Si基板
2　SiO_2膜
3　SiN膜
4　SiO_2膜
5　SOG
6　HTO膜
7　SiO_2膜
8　ゲートSiO_2膜
9　ゲート電極

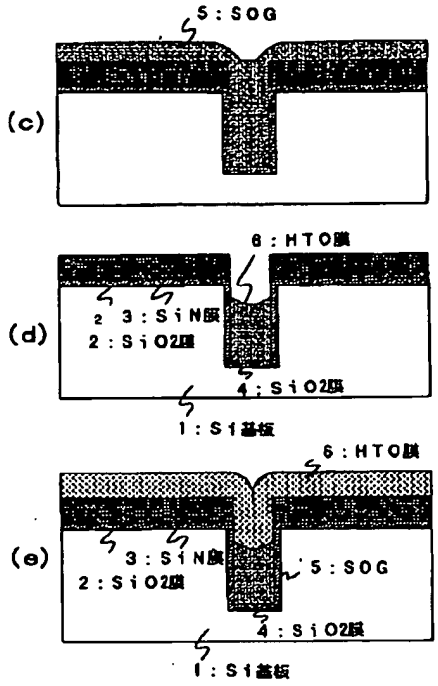
【図6】



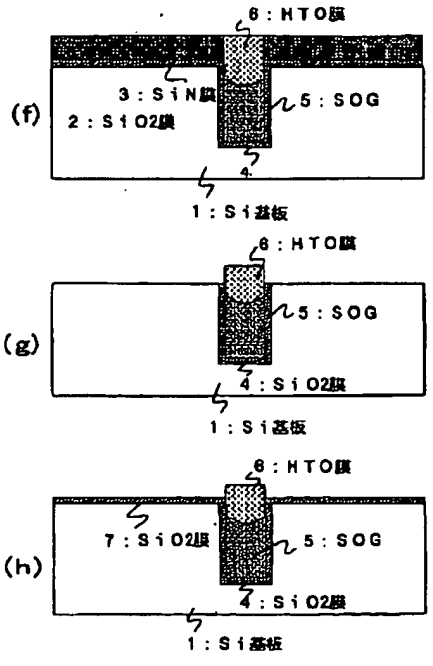
【図1】


3：SiN膜
2：SiO2膜
(a)
1：Si基板
3：SiN膜
2：SiO2膜
(b)
4：SiO2膜
1：Si基板

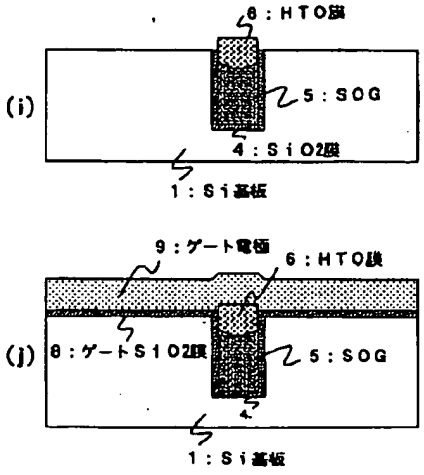
【図2】


5：SOG
(c)
6：HTO膜
3：SiN膜
2
2：SiO2膜
(d)
4：SiO2膜
1：Si基板
6：HTO膜
3：SiN膜
2：SiO2膜
(e)
5：SOG
4：SiO2膜
1：Si基板

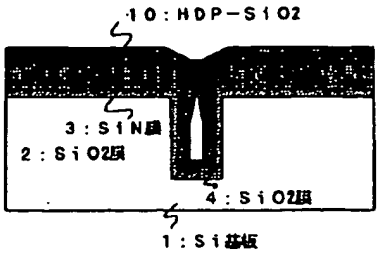
【図3】


6：HTO膜
3：SiN膜
2：SiO2膜
(f)
5：SOG
4
1：Si基板
6：HTO膜
5：SOG
(g)
4：SiO2膜
1：Si基板
6：HTO膜
7：SiO2膜
5：SOG
(h)
4：SiO2膜
1：Si基板

【図4】


6：HTO膜
5：SOG
(i)
4：SiO2膜
1：Si基板
9：ゲート電極
6：HTO膜
8：ゲートSiO2膜
5：SOG
(j)
4
1：Si基板

【図5】



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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

JP 2000-114,362

CLAIMS

[Claim(s)]
[Claim 1] It is the manufacture approach of the semiconductor device which embeds by SOG to the middle of the depth direction of a trench, and is characterized by the upper part of a trench performing embedding with an oxide film in case embedding by the oxide film of trench component part separation is performed in the manufacture approach of a semiconductor device of having the shape of a trench equation which is separable.
[Claim 2] The approach according to claim 1 the oxide film of the upper part of said trench is the HTO film or LTO film.
[Claim 3] The approach according to claim 1 said SOG film is the inorganic SOG film, the organic SOG film, or HSQ (Hydrogen-Silsesquioxane) film.

[Translation done.]

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of the semiconductor device improved so that the shape of a good trench equation which is separable might be acquired in detail about the manufacture approach of a semiconductor device of having a trench separation process.
[0002]
[Description of the Prior Art] By the manufacture approach of a semiconductor device that this invention is related, it is one of the important elements that the shape of a good trench equation which is separable is acquired.
[0003] For this object, embedding nature is comparatively good and there is usually an approach using HDP-CVD as an approach of obtaining the trench embedding oxide film of the membraneous quality near the thermal oxidation film. However, by this approach, when embedding of the trench of a three or more-aspect ratio high aspect ratio is performed by trench separation width of face of 200nm or less, sufficient embedding nature will not be obtained like drawing 5 , but aggravation of an isolation property will be caused.
[0004] Moreover, there is the approach of forming an oxide film as an approach of forming an oxide film with sufficient embedding nature using SOG which is the spreading film. According to this approach, although the embedding of the trench of the above high aspect ratios becomes possible, as shown in drawing 6 , the fault that a large level difference arises is between a trench and other parts.
[0005] Furthermore, the trench separation approach of a semiconductor device is indicated by JP,7-077231,B. In this well-known approach, in order to embed the large trench of an aspect ratio without a clearance, after carrying out, carrying out opening of the trench pattern to those film, excavating a trench for a nitride on a mask and oxidizing a trench front face, etchback is carried out and SOG is made into spreading and the structure where SOG embeds a trench to near the trench front face, in the growth-on substrate back by the underlay oxide film and the nitride. Then, the substrate with a small level difference which has trench separation is obtained by removing the oxide film and nitride which the HTO film with sufficient wet etching resistance was grown up by CBD, and prepared it in early stages, and oxidizing a substrate front face.
[0006]
[Problem(s) to be Solved by the Invention] However, since the SOG film has weak wet etching resistance, it is greatly etched like drawing 3 by the wet etching process in a device process, the configuration of trench separation gets worse, and it has an adverse effect on a component property. Moreover, the SOG film is film containing many impurities, such as a metal, and a possibility of doing the adverse effect to a gate oxidation process etc. is shown in a trench front face in the condition that the SOG film is unreserved.
[0007] The main objects of this invention are to offer the manufacture approach of the semiconductor device which forms the trench separation with sufficient embedding nature.
[0008] Etching resistance forms strong trench separation and other objects of this invention have it in

offering the manufacture approach of a semiconductor device with high process stability.
[0009]
[Means for Solving the Problem] The description of this invention is in the embedding process of trench isolation to form the oxide film which used SOG to the middle of the depth direction of a trench, and form the embedding of the upper part of a trench with the oxide film by the CVD method.
[0010] That is, in the manufacture approach by this invention, in case embedding by the oxide film of trench component part separation is performed, it embeds by SOG to the middle of the depth direction of a trench, and the upper part of a trench performs embedding with SiO2 film, for example, the HTO film, as an oxide film by CVD.
[0011] Thus, by performing embedding of the trench upper part using SOG, the duty which prevents the configuration aggravation by the wet etching in the inside of a device process by it becoming easy to perform embedding of the high trench of an aspect ratio, and forming the embedding of the trench upper part by CVD film, such as HTO film with sufficient membraneous quality, especially wet etching resistance, is achieved.
[0012] Therefore, the effectiveness that the trench separation with sufficient embedding nature with high process stability can also realize a trench with a high aspect ratio is acquired.
[0013]
[Embodiment of the Invention] This invention is explained with reference to a drawing. Drawing 1 (a) thru/or drawing 4 (j) show the process sectional view in the gestalt of 1 operation of this invention.
[0014] First, on the Si substrate 1, SiO2 film 2 is formed by the thickness of 10nm by thermal oxidation, and the SiN film 3 is formed by the thickness of 150nm with a CVD method. And the SiN film 3, SiO2 film 2, and the Si substrate 1 are etched by anisotropic etching using a lithography process, respectively, and the slot of trench separation is formed in width of face of 200nm, and a depth of 500nm (drawing 1 (a)).
[0015] And for etching damage relaxation, SiO2 film 4 is formed in the interior of a trench by thermal oxidation (drawing 1 (b)).
[0016] Subsequently, an SOG solution is applied, for example, BEKU is performed at 400 degrees C, and the SOG film 5 is formed (drawing 2 (c)). Since the SOG film 5 is formed by applying a solution in this way, it is embedded also to the interior of the high trench of an aspect ratio like this example, and can improve [a sex] film formation. Next, by Mr. about 100nm Fukashi, anisotropy dry etching performs etchback of the SOG film 5 from Si substrate front face (drawing 2 (d)).
[0017] Next, embedding is performed by forming the so-called HTO film 6 by performing oxide-film formation by the thickness of 200nm by performing CVD for 100nm of upper parts of the slot on the trench at an about 800-degree C elevated temperature using silane system gas (drawing 2 (e)).
[0018] The wet etching resistance of this HTO film 6 is also high, and it is known for being hard to mix a metal impurity etc. And the excessive HTO film 6 on SiN is removed by CMP (drawing 3 (f)).
[0019] Subsequently, although the SiN film 3 and SiO2 film 2 are removed (drawing 3 (g)), and SiO2 film 7 which serves as a mask of a well or the ion implantation of channel formation by thermal oxidation is formed (drawing 3 (h)), and it omits by wet etching since it is easy by a diagram After forming a well and a channel by the ion implantation, SiO2 film 7 is removed by wet etching (drawing 4 (i)), and the gate electrode 9 is formed of thermal oxidation by the polish recon by gate SiO2 film 8 and the CVD method (drawing 4 (j)).
[0020] After this, patterning of a gate electrode will be performed by the well-known approach, a source drain will be formed, and an MOS device will be formed through a wiring process.
[0021] In such a manufacture approach, since the lower part of a trench is embedded by SOG and the upper part is embedded for example, by the HTO film with the CVD method, and the high trench of an aspect ratio like this example could also be embedded good and it has covered by the HTO film with high wet etching resistance, film decrease of the trench oxide film in a process is also small, and a trench configuration good for this reason is acquired. Furthermore, since SOG is capped, the effectiveness that the effect of the gate oxidation process on the impurity in SOG etc. can also be prevented is brought about. Thereby, the film with high wet etching resistance can be formed.

[0022] In the gestalt of the above-mentioned operation, if the height of wet etching resistance is obtained instead of the HTO film, the so-called LTO film which made growth temperature low may be used. Moreover, it is known that the film with high wet etching resistance will be obtained, and this may be used for the oxide film which also formed plasma CVD by HDP(High Density Plasma) CVD instead of being HTO. Furthermore, ** inorganic [SOG] and organic [SOG] may be used for the SOG film, and the spreading film of a low dielectric constant like HSQ (Hydrogen-Silsesquioxane) may be used for it.
[0023]
[Effect of the Invention] As explained above, in the manufacture approach of the semiconductor device of this invention, by performing embedding of the trench upper part using SOG, it is it becoming easy to perform embedding's of the high trench of an aspect ratio, and forming the embedding of the trench upper part by CVD film, such as HTO film with sufficient membraneous quality, especially wet etching resistance, and the duty which prevents the configuration aggravation by the wet etching in the inside of a device process is achieved.
[0024] Therefore, the effectiveness that the trench separation with sufficient embedding nature with high process stability can also realize a trench with a high aspect ratio is acquired.

[Translation done.]

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the manufacture approach of the semiconductor device improved so that the shape of a good trench equation which is separable might be acquired in detail about the manufacture approach of a semiconductor device of having a trench separation process.

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PRIOR ART

[Description of the Prior Art] By the manufacture approach of a semiconductor device that this invention is related, it is one of the important elements that the shape of a good trench equation which is separable is acquired.
[0003] For this object, embedding nature is comparatively good and there is usually an approach using HDP-CVD as an approach of obtaining the trench embedding oxide film of the membraneous quality near the thermal oxidation film. However, by this approach, when embedding of the trench of a three or more-aspect ratio high aspect ratio is performed by trench separation width of face of 200nm or less, sufficient embedding nature will not be obtained like drawing 5 , but aggravation of an isolation property will be caused.
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[0005] Furthermore, the trench separation approach of a semiconductor device is indicated by JP,7-077231,B. In this well-known approach, in order to embed the large trench of an aspect ratio without a clearance, after carrying out, carrying out opening of the trench pattern to those film, excavating a trench for a nitride on a mask and oxidizing a trench front face, etchback is carried out and SOG is made into spreading and the structure where SOG embeds a trench to near the trench front face, in the growth-on substrate back by the underlay oxide film and the nitride. Then, the substrate with a small level difference which has trench separation is obtained by removing the oxide film and nitride which the HTO film with sufficient wet etching resistance was grown up by CBD, and prepared it in early stages, and oxidizing a substrate front face.

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EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, in the manufacture approach of the semiconductor device of this invention, by performing embedding of the trench upper part using SOG, it is it becoming easy to perform embedding's of the high trench of an aspect ratio, and forming the embedding of the trench upper part by CVD film, such as HTO film with sufficient membraneous quality, especially wet etching resistance, and the duty which prevents the configuration aggravation by the wet etching in the inside of a device process is achieved.
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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, since the SOG film has weak wet etching resistance, it is greatly etched like drawing 3 by the wet etching process in a device process, the configuration of trench separation gets worse, and it has an adverse effect on a component property. Moreover, the SOG film is film containing many impurities, such as a metal, and a possibility of doing the adverse effect to a gate oxidation process etc. is shown in a trench front face in the condition that the SOG film is unreserved.
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MEANS

[Means for Solving the Problem] The description of this invention is in the embedding process of trench isolation to form the oxide film which used SOG to the middle of the depth direction of a trench, and form the embedding of the upper part of a trench with the oxide film by the CVD method.
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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] (a) and (b) are a process sectional view in the gestalt of 1 operation of this invention.
[Drawing 2] (c) - (e) is the process sectional view of the process performed following the process of drawing 1 (a).
[Drawing 3] (f) - (h) is the process sectional view of the process performed following the process of drawing 2 (e).
[Drawing 4] (i) and (j) are the process sectional view of the process performed following the process of drawing 3 (h).
[Drawing 5] The sectional view showing the trench embedding oxide film obtained by the conventional approach.
[Drawing 6] The sectional view showing the trench embedding oxide film obtained by other conventional approaches.
[Description of Notations]
1 Si Substrate
2 SiO2 Film
3 SiN Film
4 SiO2 Film
5 SOG
6 HTO Film
7 SiO2 Film
8 Gate SiO2 Film
9 Gate Electrode

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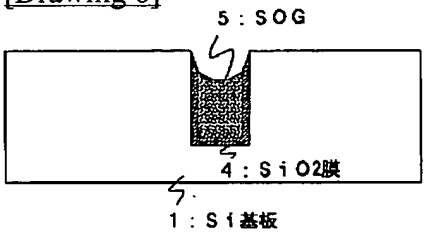
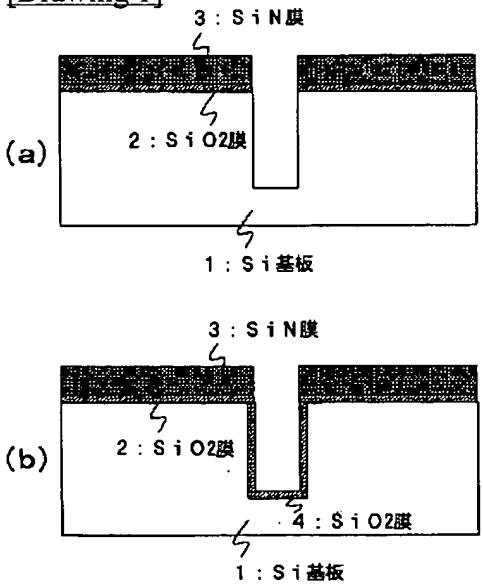
DRAWINGS

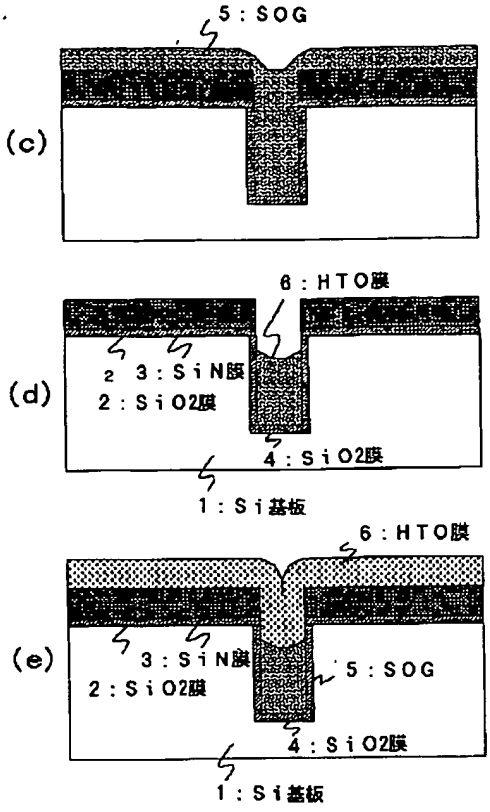
[Drawing 6]



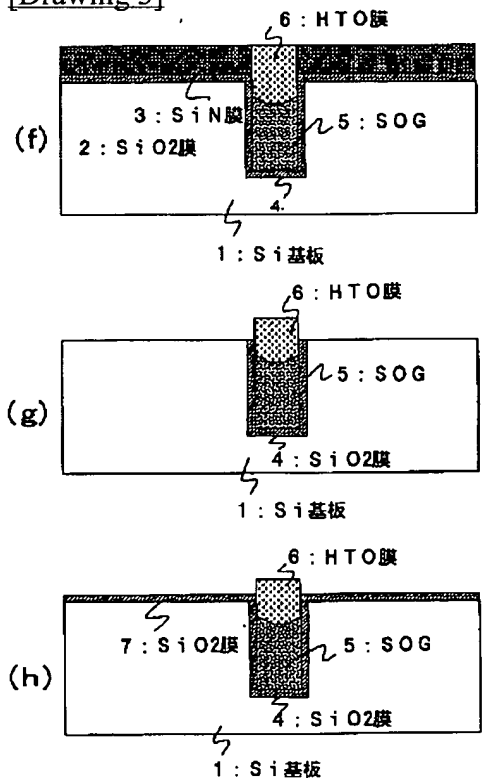
[Drawing 1]



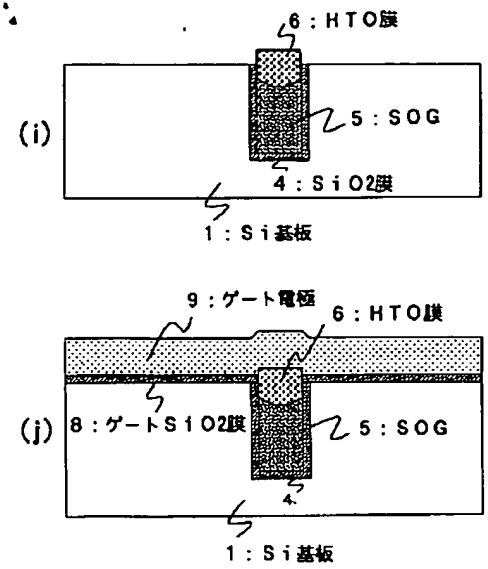
[Drawing 2]



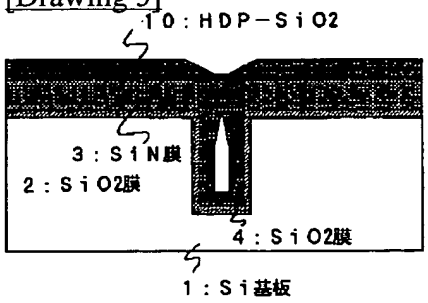
[Drawing 3]



[Drawing 4]



[Drawing 5]



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